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EXAMINER	
MOORE, PATRICK M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,817	RIESCHL ET AL.	
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 & 25-34* is/are rejected.

7)☐ Claim(s) *24 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 33 & 34** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. **Claim 33 & 34** recite the limitations "said second look-up table" in Line 2 of both Claims. There is insufficient antecedent basis for this limitation in the Claims. *Examiner assumes that* ***Claim 30*** *should include the limitation "first determining whether a page address has been allocated to said main memory address* **through use of a second lookup table**,*" in lieu of the recited "first determining whether a page address has been allocated to said main memory address," limitation.*

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-23 & 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsuchiya et al.** (US Patent # 5,530,823) in view of **Hellestrand et al.** (US Patent # 6,230,114), herein **Tsuchiya** and **Hellestrand**, respectively.

a. **As per Claim 1**, **Tsuchiya** discloses a large computer memory, wherein said large computer memories are defined by a plurality of memory addresses, wherein each of said plurality of addresses contains data, and wherein said large computer memories are large enough to prevent simulation via the use of one-to-one memory to file addressing for all of said plurality of memory addresses **[Column 1, Lines 22-24]**, wherein said main memory comprises: a memory cache **[Figure 1, #12-14]**; and a processor operable with said memory cache **[Figure 1, #11 & Column 2, Line 65 – Column 3, Line 2]**, wherein said processor operates under instructions to move data contained in frequently used memory addresses of said plurality of memory addresses to said memory cache on a fast memory access basis **[Figure 1, #19, 21 & 23]** and under instructions to move data contained in infrequently used memory addresses of said plurality of memory addresses to said memory cache on a slow memory access basis **[Figure 1, #17, 24 & Column 3, Lines 14-44]**.

b. **Tsuchiya** does not expressly disclose a memory simulator to simulate the main memory. However, **Hellestrand** discloses a main memory simulator for simulating large computer memories **[Column 4, Lines 43-62]**. **Tsuchiya** *and* **Hellestrand** *are analogous art because they are from the same field of endeavor: computer hardware optimization. At the time of invention, it would*

have been obvious for one of ordinary skill in the art to combine the memory simulator, as taught by **Hellestrand**, *with the frequency-based lookup tables, as taught by* **Tsuchiya**. *The suggestion/motivation for doing so would have been for the benefit of testing interactions between a processor with memory elements of an integrated circuit board, before the integrated circuit board is fabricated. Hellestrand discloses that this advantage would "clearly save time and money"* **[Column 1, Line 39]**.

c. **As per Claim 2**, **Tsuchiya** further discloses the simulator of claim 1, wherein said fast memory access comprises the utilization of a set of fast lookup tables to directly obtain a page address **[Figure 1, #23]** that has been allocated to the frequently used memory address **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

d. **As per Claim 3**, **Tsuchiya** further discloses the simulator of claim 1, wherein said slow memory access comprises the utilization of a slow lookup table to first determine if a page address has been allocated to the infrequently used memory address and to then obtain the allocated page address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

e. **As per Claim 4**, **Tsuchiya** further discloses the simulator of claim 2, wherein said slow memory access comprises the utilization of a slow lookup table to determine if a page address has been allocated to the infrequently used memory address and the obtainment of said page address if allocated **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

f. **As per Claim 5**, **Tsuchiya** further discloses the simulator of claim 1, wherein the movement of data is achieved through a page transfer **[Column 1, Lines 37-44]**.

g. **As per Claim 6**, **Hellestrand** discloses a main memory simulator for simulating large computer memories. **Tsuchiya** discloses that said large computer memories are defined by a plurality of memory addresses, wherein each of said plurality of addresses contains data, and wherein said large computer memories are large enough to prevent simulation via the use of one-to-one memory to file addressing for all of said plurality of memory addresses, wherein said simulator comprises: means for storing data **[Column 3, Lines 2-25]**; means for processing instructions, wherein said means for processing instructions is in communication with said means for storing data **[Figure 1, #15 & Column 3, Lines 2-13]**; and means for providing instructions to said means for processing instructions, wherein said means for providing instructions provides the instruction to transfer data by identifying a memory address of said data, wherein said memory address comprises at least one of said plurality of memory addresses **[Column 3, Lines 14-25]**; wherein said means for processing instructions processes said instruction to transfer data by determining if said memory address of said data is a frequently or infrequently accessed memory address **[Column 3, Lines 14-44]**, and by transferring said data to said means for storing via a fast memory access scheme if said data is a frequently accessed memory address or by transferring said data to said means

for storing via a slow memory access scheme is an infrequently addressed memory address **[Column 3, Lines 14-44]**. *As above, identical motivation exists to combine* **Hellestrand** *with* **Tsuchiya**.

h. **As per Claim 7**, **Tsuchiya** further discloses the simulator of claim 6, wherein fast memory access scheme comprises utilizing a set of fast lookup tables **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

i. **As per Claim 8**, **Tsuchiya** further discloses the simulator of claim 7, wherein said fast lookup tables enable said means for processing to directly obtain a page address corresponding to said frequently accessed address **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

j. **As per Claim 9**, **Tsuchiya** further discloses the simulator of claim 6, wherein said slow memory access scheme comprises utilizing a slow lookup table **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

k. **As per Claim 10**, **Tsuchiya** further discloses the simulator of claim 9, wherein said slow lookup table enables said means for processing to first determine if a page address has been allocated to said infrequently addressed memory address and then obtaining the allocated page address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

l. **As per Claim 11**, **Tsuchiya** further discloses the simulator of claim 6, wherein said transferring of data is achieved through a page transfer **[Column 1, Lines 37-44]**.

m. **As per Claim 12**, **Hellestrand** discloses a method for simulating large computer memories. **Tsuchiya** discloses that said large computer memories are defined by a plurality of memory addresses, wherein each of said plurality of addresses contains data, and wherein said large computer memories are large enough to prevent simulation via the use of one-to-one addressing for all of said plurality of memory addresses, the method comprising: obtaining a request for transfer of data within at least one of said plurality memory addresses, wherein said request identifies the memory address of said at least one of said plurality of memory addresses containing said data **[Column 3, Lines 25-44]**; determining whether the requested memory address is a frequently requested memory address or whether the requested memory is an infrequently requested memory address **[Column 3, Lines 14-25]**; if the determination reveals a frequently requested memory address, then using a fast memory access scheme to transfer the data within said frequently requested memory address **[Figure 1, #19, 21 & 23]**; and if the determination reveals an infrequently requested memory address, then using a slow memory access scheme to transfer the data within said infrequently requested memory address **[Figure 1, #17, 24 & Column 3, Lines 14-44]**. *As above, identical motivation exists to combine* **Hellestrand** *with* **Tsuchiya**.

n. **As per Claim 13**, **Tsuchiya** further discloses the method of claim 12, wherein said fast memory access scheme comprises utilizing a set of fast lookup tables **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

o. **As per Claim 14**, **Tsuchiya** further discloses the method of claim 13, wherein said fast lookup tables enable direct obtainment of a page address corresponding to said frequently accessed address **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

p. **As per Claim 15**, **Tsuchiya** further discloses the method of claim 12, wherein said slow memory access scheme comprises utilizing a slow lookup table **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

q. **As per Claim 16**, **Tsuchiya** further discloses the method of claim 15, wherein said slow lookup table first enables determining if a page address has been allocated to said infrequently addressed memory address and then enables obtaining the allocated page address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

r. **As per Claim 17**, **Tsuchiya** further discloses the method of claim 12, wherein said transfer of data comprises a page transfer **[Column 1, Lines 37-44]**.

s. **As per Claim 18**, **Hellestrand** discloses a memory simulation system for simulating a main memory of a computer. **Tsuchiya** discloses that the spaces of memory within said main memory are defined by a main memory address, the system comprising: a plurality of files, wherein said files include a fast look-up table and a slow look-up table **[Column 3, Lines 14-44]**, wherein said fast look-up table is operable to directly obtain a page address that has been allocated to said main memory address **[Figure 1, #19, 21 & Column 3, Lines 9-13]**, and wherein said slow look-up table is operable to first determine if a page

address has been allocated to said main memory address and if a page address has been allocated to said main memory address, to obtain the allocated page address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**; a cache, wherein said cache includes a buffer **[Column 3, Lines 5-9]**; and an interface **[Figure 1, #16]**, wherein said interface receives a request for transfer of main memory between at least one of said plurality of files and said buffer **[Column 3, Lines 14-25]**, wherein said request is made through input of said main memory address to said interface, and wherein in response to said request said interface performs a page transfer between said at least one of said plurality of files and said buffer according to the page address that has been allocated to said main memory address via said fast look-up table or said slow look-up table **[Column 1, Lines 37-44 & Column 3, Lines 1-44]**. *As above, identical motivation exists to combine* **Hellestrand** *with* **Tsuchiya**.

t. **As per Claim 19**, **Hellestrand** further discloses the system of claim 18, wherein said plurality of files further include a last access look-up table, wherein said last access look-up table includes a last memory address accessed and the page address allocated to said last memory address accessed **[Column 9, Lines 16-34]**. *Examiner understands that storing the simulator's information about "the last event" must inherently include storing the last accessed memory and page addresses.*

u. **As per Claim 20**, **Hellestrand** further discloses the system of claim 18, wherein upon said interface performing a page transfer, said main memory

address represented by the page is used to search a breakpoint list, and wherein upon finding that a word within said page has a breakpoint set as indicated by the search of said breakpoint list, a breakpoint flag within a page descriptor of said page is set **[Column 15, Line 64 – Column 16, Line 14]**. *Examiner understands that highlighting the current instruction after encountering a breakpoint, as taught by* **Hellestrand** *in* **Column 16, Line 8**, *is functionally equivalent to flagging the indicated page location of the breakpoint.*

v. **As per Claim 21**, **Hellestrand** further discloses the system of claim 18, wherein both said fast look-up table and said slow lookup table are savable into a finite number of files **[Column 15, Line 64 – Column 16, Line 14]**. *Examiner understands that stopping the system at a breakpoint must inherently save all variable values, which would include both tables claimed by Applicant, in order to allow user inspection of such variable values.*

w. **As per Claim 22**, **Hellestrand** further discloses the system of claim 21, wherein said fast look-up table and said slow look-up table are restorable from the saved files enabling a previously stopped simulation to continue **[Column 15, Line 64 – Column 16, Line 14]**. *Examiner further believes that "single stepping" the system through single instructions indicates that the previously saved variable values must inherently have been restored, in order to continue operating with such variables.*

x. **As per Claim 23**, **Tsuchiya** further discloses the system of claim 18, wherein said fast look-up table is used to obtain a page address for memory that is

accessed frequently and wherein said slow look-up table is used to obtain a page address for memory that is accessed infrequently **[Column 3, Lines 14-44]**.

y. **As per Claim 25**, **Hellestrand** discloses a memory simulation system for simulating main memory of a computer. **Tsuchiya** discloses that the spaces of memory within said main memory are defined by a main memory address, the system comprising: means for receiving a data transfer request, wherein said data transfer request is defined by a main memory address **[Column 3, Lines 14-44]**; means for determining the frequency of use of said main memory address **[Column 3, Lines 14-44]**; means for obtaining a page address corresponding to said main memory address **[Column 3, Lines 14-44]**, wherein said means for obtaining includes: means for obtaining a page address corresponding to said main memory address when said main memory address has been determined to be frequently used **[Figure 1, #19, 21 & Column 3, Lines 9-13]**; and means for obtaining a page address corresponding to said main memory address when said main memory address has been determined to be infrequently used **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**; means for transferring data to a memory location, wherein said transferring of data comprises a page transfer in accordance with the obtained page address **[Column 1, Lines 37-44]**. *As above, identical motivation exists to combine* **Hellestrand** *with* **Tsuchiya**.

z. **As per Claim 26**, **Tsuchiya** further discloses the system of claim 25, wherein said means for obtaining the page address of the frequently used main memory

address comprises a set of fast lookup tables **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

aa. **As per Claim 27**, **Tsuchiya** further discloses the system of claim 26, wherein said fast lookup tables enable said means for obtaining to directly obtain the page address of the frequently used main memory address **[Figure 1, #19, 21 & Column 3, Lines 9-13]**.

bb. **As per Claim 28**, **Tsuchiya** further discloses the system of claim 25, wherein said means for obtaining the page address of the infrequently used main memory address comprises a slow lookup table **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

cc. **As per Claim 29**, **Tsuchiya** further discloses the system of claim 28, wherein said slow lookup table enables said means for obtaining to first determine if a page address has been allocated to said main memory address and then to obtain that allocated pages address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**.

dd. **As per Claim 30**, **Hellestrand** discloses a method of memory transfer for use in simulating a main memory. **Tsuchiya** discloses that the spaces of memory within said main memory are defined by a main memory address, the method comprising: obtaining a main memory address, wherein said main memory address indicates a request for a main memory transfer between a file and a cache buffer **[Column 3, Lines 5-9]**; determining if said main memory address comprises memory that is accessed frequently or infrequently; if said main

memory address comprises memory that is accessed frequently, directly obtaining a page address that has been allocated to said main memory address through use of a first look-up table **[Figure 1, #19, 21 & Column 3, Lines 9-13]**; if said main memory address comprises memory that is accessed infrequently, first determining whether a page address has been allocated to said main memory address, then obtaining the page address that has been allocated to said main memory address **[Figure 1, #17, 24, 15 & Column 3, Lines 14-25]**; transferring the requested main memory between said file and said cache buffer via a page transfer that utilizes the page address allocated to said main memory address **[Column 1, Lines 37-44]**. *As above, identical motivation exists to combine* **Hellestrand** *with* **Tsuchiya**.

ee. **As per Claim 31**, **Hellestrand** further discloses the method of claim 30, further comprising the step of saving the last main memory address accessed and the corresponding page address **[Column 9, Lines 16-34]**.

ff. **As per Claim 32**, **Hellestrand** further discloses the method of claim 30, further comprising the step of searching a breakpoint list, wherein upon discovering that a word within the transferred page has a breakpoint set as indicated by the search of said breakpoint list, setting a breakpoint flag within a page descriptor of the transferred page **[Column 15, Line 64 – Column 16, Line 14]**.

gg. **As per Claim 33**, **Hellestrand** further discloses the method of claim 30, further comprising the step of saving said first look-up table and said second

look-up table into a number of finite files **[Column 15, Line 64 – Column 16, Line 14]**.

hh. **As per Claim 34**, **Hellestrand** further discloses the method of claim 33, further comprising the step of restoring said first lookup table and said second look-up table to continue a previously stopped simulation **[Column 15, Line 64 – Column 16, Line 14]**.

Allowable Subject Matter

4. Claims 24 & 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Masuda et al. (US Patent # 5,278,962) discloses an address conversion system, which translates a virtual address and fetches page data from an actual memory location. Miyadira et al. (US Patent # 4,769,770) discloses address conversion that determines if a logical address lies within a predetermined address range. Masuda et al. (US Patent # 4,954,942) discloses an address conversion buffer employing breakpoints in a hardware emulation system for debugging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMM

Mano Padmanabhan
5/1/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER